Remarks/Arguments

There are no amendments to the specification or the drawings herein.

In the claims, Claims 1-25 remain and are pending in the application. Claims 12-20 are allowed. Claims 1-8, 11 and 21-25 are rejected and Claims 9 and 10 are objected to. New Claims 26 and 27 are added. Reconsideration is respectfully requested.

The Examiner made final a rejection of Claims 1, 3-8, 11 and 21-25 under 35 U.S.C. 102(b) as being anticipated by Patel et al., U.S. Patent No. 6,025,737 (hereinafter 'Patel et al.').

In a previous Response/Amendment, filed December 21, 2005 (hereinafter 'Previous Response'), Applicant traversed the rejection of Claims 1, 3-8, 11 and 21-25 in view of Patel et al. on the grounds that a *prima facie* case of anticipation had not been established. Herein, Applicant once again traverses the rejection of Claims 1, 3-8, 11 and 21-25 in view of Patel et al. for lack of *prima facie* case of anticipation with respect to Patel et al. In particular, the Examiner has failed to show that Patel et al. disclose, explicitly or implicitly, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983)), and also has failed to show that Patel et al. disclose the claimed elements "arranged as in the claim" (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)) as required by the Federal Circuit for *prima facie* anticipation under 35 U.S.C. 102.

In the Previous Response, Applicant argued that Patel et al. do not disclose or even suggest each and every element recited in at least Applicant's independent base Claims 1, 6, and 21. In part, Applicant argued that Patel et al. do not disclose a "bias generator" or an output thereof (including "a bias voltage output signal"), as defined by Applicant's specification and recited in Applicant's claims. Instead, Patel et al. disclose an inverting input buffer that is not and cannot be equivalent to Applicant's claimed bias generator. In particular, the inverting buffer disclosed by Patel et al. ***is incapable*** of, "producing as an output signal a bias voltage V_{bias}" having "a magnitude that is selectable from among a set of available magnitudes", as defined by Applicant for the "bias generator" and the "bias generator output signal" recited in Applicant's

claims (see Applicant's specification, Page 5, line 30, through Page 6, line 1, for example). The Examiner has continued to contend, "Patel et al. discloses a bias generator [1050, 1055] ... comprising: an output (To core) of the bias generator". However, according to Patel et al., the '[1050, 1055]' is an inverter input buffer and the 'To Core' signal is a digital signal. In fact, the "To Core" signal produced by the inverter input buffer, according to Patel et al., ***is and can only*** be a digital inverse of a logic level appearing on I/O pin 820. As such, there can be no "set of available magnitudes of a bias voltage output signal at the [bias generator] output", as recited in Applicant's claims. Applicant respectfully directs the Examiner to the Previous Response for a complete discussion of the myriad or additional differences between the 'inverting input buffer' according to Patel et al. and Applicant's claimed "bias generator" and their respective output signals.

In a ***Response to Arguments*** section of the present Office Action (hereinafter 'Present Action') on page 8, the Examiner disagreed with Applicant's arguments contending, "a bias signal is a signal uses [*sic*] to control or drive a circuit". The Examiner provided no source for the offered definition of "bias signal" and made no attempt to reconcile the Examiner's offered definition with the clearly different definition of "bias voltage output signal" provided by Applicant's specification. The Examiner concluded, "Patel [1050 and 1055] clearly discloses a bias signal 'To Core', because the signal 'To Core' generating [*sic*] by 1050 and 1055 is using [*sic*] to drive and control the Core; thereby 1050/1055 is a generator".

Applicant respectfully and strongly objects to the Examiner's flagrant disregard for Applicant's definition and usage of the claim terms, "bias generator", "bias voltage output signal" in Applicant's specification as originally filed in maintaining the rejection. The Examiner respectfully ***may not*** simply fabricate and employ ***without explicit support in the prior art*** any definition of Applicant's claim terms that may advantageously provide support to the Examiner's rejection. The Examiner is reminded that in establishing a *prima facie* case of anticipation, "the trier of fact must identify the elements of the claims, ***determine their meaning in light of the specification and prosecution history***, and identify corresponding elements disclosed in the allegedly anticipating reference." (***emphasis*** added) *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ

481, 485 (Fed. Cir. 1984). It respectfully appears that the Examiner has refused to ***determine the meaning*** of Applicant's recited "elements of the claims" "in light of the specification and prosecution history", which is flagrantly contrary to the Federal Circuit in establishing a *prima facie* case of anticipation.

Applicant also respectfully reminds the Examiner that as stated in the MPEP §2173.01, "[a] ***fundamental*** principle contained in 35 U.S.C. 112, second paragraph is that applicants are their own lexicographers. They can define in the claims what they regard as their invention essentially in whatever terms they choose so long as any special meaning assigned to a term is clearly set forth in the ***specification***" (***emphasis*** added). Moreover, "[c]onsistent with the well-established axiom in patent law that a patentee or applicant is free to be his or her own lexicographer, a patentee or applicant may use terms in a manner contrary to or inconsistent with one or more of their ordinary meanings if the written description clearly redefines the terms. See, e.g., *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999)" (MPEP §2173.05(a)(III)). Thus, during examination, while the claims must be interpreted as broadly as their terms reasonably allow, it is not only permissible but often necessary for the Examiner to use definitions from the specification for terms appearing in the claims in order to properly interpret claim language (see MPEP §2111.01). Furthermore, "[w]here an ***explicit definition is provided*** by the applicant for a term, that definition ***will control interpretation*** of the term as it is used in the claim. *Toro Co. v. White Consolidated Industries Inc.*, 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999) (***emphasis*** added)" MPEP, 2111.01 *Plain Meaning*, Part III. Thus, the Examiner is ***obliged to employ Applicant's definition*** of claim terms when an explicit definition is provided pursuant to Applicant's statutory right to be his/her own lexicographer and pursuant to that held by the Federal Circuit (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, cited *supra*).

Regarding the Examiner's definition, a more common and consistent definition of the term "bias voltage" is a voltage (typically DC) applied to a component or device to establish a reference level or operating point of the device. More particularly, as employed in weak write testing of a static random access memory (SRAM), the term "bias voltage" applies to a programmable voltage that,

"facilitates adjusting or modulating a strength of the weak write pull-down transistor", the bias voltage compensating for, "for manufacturing related variations in a performance of the weak write pull-down transistor" (Applicant's specification, Page 5, lines 17-19). In contrast, the "To Core" signal according to Patel et al. is neither a programmable voltage nor a voltage that is applied to a component or device to establish a reference level or operating point of the device. Also, in the inverter input buffer circuit (i.e., 1050, 1055) according to Patel et al., the "To Core" signal may take on either of two predetermined (but not programmable) voltages, the voltage being entirely determined by the supply voltages VCCQ or VCCINT and VSSQ applied to the circuit. Moreover, the inverter input buffer does not 'bias' a component or device with the "To Core" but acts as a data interface that passes digital data from the I/O pin 820 to a core of the integrated circuit.

In the Previous Response, Applicant further argued that Patel et al. do not disclose, "means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal programming", as recited, in part, in Applicant's Claim 1. Similarly, Patel et al. fail to disclose, "a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal at the bias generator output when metal programmed", or "metal programming the metal-programmable transistor ... to modify the available magnitudes of the set", of the bias voltage output signal, as recited in base Claims 6 and 21, respectively. Applicant pointed out that according to Patel et al., the "metal options" associated with transistors 1060, 1062, 1064, and 1066 adjust a "trip point" of the disclosed inverting input buffer. The disclosed "metal options" ***do not*** affect a level of an output signal (e.g., "To Core") of the inverting buffer according to Patel et al.

The Examiner, in the ***Response to Arguments*** section of the Present Action (pages 8-9) disagreed and contended, "Patel's [1060, 1064] (Col. 15 lines 50-52 and 62-64) clearly disclose means (See Fig. 10D and 10E for disclosing adjusting the bias signal "To Core) for adjusting a set of available magnitudes (Fig. 10,D, [*sic*] 10B) at the output of a bias voltage output signal (To Core) at the output using metal programming (Col. 15 lines 48-53)". The Examiner further contended, "Fig. 10C of Patel clearly discloses a metal programmable transistor (1060, 1064, 1062, 1066) that

adjusts a set of available magnitudes of a bias voltage output signal (To Core) at the bias generator (1050, 1055) when metal programmed (10E, 10D)".

It is respectfully submitted that the Examiner's contention with respect to that disclosed by Patel et al., restated verbatim above, is as incomprehensible as it is stunning. Applicant is respectfully at a loss as to how the Examiner can so blatantly misconstrue and misapply a reference in an attempt to support the instant rejection. With all due respect, any undergraduate electrical engineering student is aware that an output voltage of an inverting buffer circuit, such as that disclosed by Patel et al., is governed solely by the supply voltages applied to the circuit (e.g., VCCQ or VCCINT and VSSQ according to Patel et al., FIG. 10B). A relative size of the transistors (e.g., 1050, 1055 plus any "metal options" provided by 1060, 1064, 1062, 1066) affect only a point in a voltage transition of an input signal applied to an input (e.g., I/O pin 820) at which an output signal (e.g., "To Core") is caused to transition from one binary state to another. The relative size of the transistors ***does not affect*** the magnitudes of the voltages associated with the binary output signal. Moreover, ***Patel et al. explicitly recognize this fact.***

For example, at Col. 15, lines 29-31, Patel et al. explicitly disclose, "[t]he ***input threshold trip point depends*** on the ratio of the relative strengths of the ratio of the pull-down transistor 1050 to the pull-down transistor 1055" (***emphasis*** added). Patel et al. further explicitly disclose, "[t]he effective size (or strength) of transistor 1050 may be adjusted using transistors 1060 and 1062", and "the effective size (or strength) of transistor 1055 may be adjusted using transistor 1064 and 1066" (Patel et al., Col. 15, lines 50-54). Patel et al. clearly disclose adjusting the size of the transistors 1050, 1055 to produce an adjustment in the trip point of the inverting input buffer and ***nothing more.***

Thus, for the Examiner to contend that Patel et al. disclose "adjusting ... bias voltage output signal at the output" of the bias generator, or anything that is remotely similar thereto, is respectfully incorrect in light of the prior art disclosure and entirely without merit. The "metal options" of Patel et al. simply ***do not and cannot*** adjust an output voltage of the inverting input buffer, contrary to the Examiner's contentions.

In the ***Response to Arguments*** section of the Present Action at page 9, the Examiner further contended, "the word 'test' is an intended of [*sic*] use because a

recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from prior art apparatus satisfying the claimed structural limitations".

Applicant respectfully points out that the disclosure by Patel et al. is far from being a prior art apparatus that satisfies the claimed structural limitations. Furthermore, Applicant's respectfully reminds the Examiner that arguments in the Previous Response with regard to "test" were directed at the Examiner's mischaracterization of the disclosure of Patel et al. in a previous Office Action mailed October 7, 2005 (hereinafter 'Previous Action'). In particular, as was discussed in the Previous Response, Patel et al. clearly do not disclose or even suggest, "a bias generator [1050, 1055] for testing (intended of use) of a static random access memory SRAM", as had been contended by the Examiner in the Previous Action.

However, while not depending on a "use" of the claimed bias generator to distinguish over the structure of Patel et al., Applicant firmly believes that the use (i.e., functional language) does place meaningful limitations on the bias generator that are consistent with 35 U.S.C. 112. Namely, the inverting input buffer disclosed by Patel et al. cannot be employed as a bias generator to test SRAM where the testing is 'weak write testing', as defined in Applicant's specification. Functional language used "to define a particular capability or purpose that is served by the recited element" in a way that sets "definite boundaries on the patent protection sought" is perfectly acceptable claim language that must be considered. (See MPEP §2173.05(g)). Thus, reference to testing SRAM using Applicant's claimed bias generator does, in fact, place meaningful structural (e.g., capability) limitations on the bias generator (see for example the preamble of Applicant's Claims 1 and 6).

In particular, electronic circuits are generally well-behaved and predictable or they would lack utility. A structure of a given electronic circuit determines what output signals that circuit can and cannot produce. When two circuits are incapable of producing the same or substantially similar output signals, those two circuits cannot be considered equivalent. As such, for structural equivalence to be established when "testing" is claimed, a hypothetical circuit that may appear in a prior art reference at least must be inherently capable of producing an output signal that is useful for the claimed testing, even if such intended use for testing is not explicitly recognized by

the reference. With out such an inherent capability, the hypothetical circuit cannot be equivalent or even similar to the claimed structure.

In light of the above, the inverter input buffer is ***incapable*** of producing an output signal that meets the criteria for weak write testing of SRAM according to Applicant's definition thereof. The absence of such a capability in and of itself precludes equivalence and by extension obviates any discussion of alleged anticipation by that circuit. Thus, contrary to the Examiner's contention, testing SRAM can and does structurally distinguish the claimed bias generator from the inverting input buffer according to Patel et al. simply by establishing capabilities of the claimed bias generator. The inverting input buffer is clearly not equivalent or even remotely similar to the bias generator claimed by Applicant.

Therefore, Applicant respectfully submits that the Examiner still has failed to establish separately for each of Applicant's base Claims 1, 6 and 21 a *prima facie* case of anticipation with respect to Patel et al. In short, Patel et al. clearly fail to disclose, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, cited *supra*) when considering Applicant's base Claims 1, 6 and 21. In particular, as detailed above, the Examiner failed to show that there is, "no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention," as required by the Federal Circuit. *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).

Having failed to establish *prima facie* anticipation of base Claims 1, 6 and 21, the Examiner similarly failed to show that dependent Claims 3-5, 7-8, 11, and 22-25 are *prima facie* anticipated by Patel et al. In particular, Claims 3-5 are dependent from and include all of the limitations of base Claim 1; Claims 7-8 and 11 are dependent from and include all of the limitations of base Claim 6; and Claims 22-25 are dependent from and include all of the limitations of base Claim 21. Hence, the rejection of base Claims 1, 6 and 21, as well as respective dependent Claims 3-8, 11 and 22-25, under 35 U.S.C. 102(b) is unsupported by facts in evidence and ***must be withdrawn***. Reconsideration and withdrawal of the rejection of Claims 1, 3-8, 11 and 21-25 under 35 U.S.C. 102(b) with respect to Patel et al. are earnestly requested.

The Examiner maintained and made final the rejection of Claim 2 under 35 U.S.C. 103(a) as being unpatentable by Patel et al. further in view of Ando, U.S. Patent No., 6,560,142 (hereinafter 'Ando'). The Examiner provided ***no response*** whatsoever to Applicant's arguments in the Previous Response regarding Applicant's traversal of the rejection. In particular, the Examiner did not comment on Applicant argument that a *prima facie* case of obviousness had not been established for the rejection of Claim 2. In light of the Examiner's silence, Applicant is at a loss as to how the Examiner can make the rejection final.

Applicant again respectfully traverses the rejection under 35 U.S.C. 103(a) on the grounds that the Examiner failed to establish and properly support a *prima facie* case of obviousness with respect to Patel et al. in view of Ando (hereinafter 'the references'). At least both of a motivation or suggestion to combine the references and a showing that the references disclose or suggest all of the claimed limitations are clearly lacking in the Examiner's rejection of Claim 2. In short, the Examiner's reasons for rejecting Claim 2 respectfully fail to meet even the minimum requirements necessary for establishing and maintaining *prima facie* obviousness with respect to the references. See for example the Previous Response and MPEP §2143.01 *Suggestion or Motivation to Modify the References*. Also see *In re Fine*, 837, F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988; *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998); *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); *Ecolochem, Inc. v. Southern Calif. Edison Co.*, 227 F.3d 1361, 1375, 56 USPQ2d 1065, 1075 (Fed. Cir. 2000); and *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

For example, as was argued by Applicant in the Previous Response, the combination of Patel et al. and Ando at least fails to disclose, "wherein the bias voltage output signal ***biases a gate of a weak write pull-down transistor of a write driver in the SRAM*** with a target magnitude predetermined for the SRAM", as recited in Applicant's Claim 2. Neither Patel et al. nor Ando disclose or suggest, "a weak write pull-down transistor". As such, the combination of Patel et al. and Ando cannot disclose all of the limitations of Applicant's Claim 2. Furthermore, reference to "WW" in Ando, relied upon by the Examiner, relates to a "write word signal" (Ando, Col. 3, lines 10-11). Such a "write word signal" is unrelated to "the bias voltage

output signal" that "biases a gate of a weak write pull-down transistor of a write driver ...", as claimed in Applicant's Claim 2. Moreover, neither Patel et al. nor Ando, whether considered separately or together, mentions or suggests a "write driver in the SRAM" or that there may be "a target magnitude [of the bias] predetermined for the SRAM", as is further recited in Claim 2. In fact, the disclosure of Ando is entirely directed to a capacitorless DRAM gain cell and does not even mention or consider SRAM or testing thereof.

As such, contrary to the Examiner's contention, the combination of Patel et al. and Ando fails to disclose or suggest all of the limitations of Claim 2, as required by the courts for establishing and supporting *prima facie* obviousness. See *In re Royka*, cited *supra*. As with a failure to provide a legitimate motivation to combine, a failure by the combined references to disclose or suggest all of the limitations of Claim 2 further defeats *prima facie* obviousness. *In re Royka*, cited *supra*.

At least for the reasons set forth above, the Examiner's rejection under 35 U.S.C. 103(a) lacks proper support for a *prima facie* case of obviousness according to the case law. Thus, the rejection of Claim 2 under 35 U.S.C. 103(a) by Patel et al. in view of Ando ***must be withdrawn***. Reconsideration and withdrawal of the rejection of Claim 2 under 35 U.S.C. 102(b) with respect to Patel et al. and Ando are earnestly requested.

Applicant once again appreciates the Examiner's acknowledgement of the allowability of Claims 9 and 10 if rewritten in independent form. In light of this acknowledgement, Applicant has added new Claims 26 and 27 for entry. New Claim 26 is allowable Claim 9 rewritten in independent form and New Claim 27 is allowable Claim 10 rewritten in independent form. Since the Examiner suggested that Claims 9 and 10 be rewritten, no new issues are raised by the added new Claims 26 and 27. Moreover, no new matter is added thereby. Applicant respectfully requests entry and allowance of new Claims 26 and 27.

In addition, Applicant appreciates the Examiner's allowance of Claims 12-20, as filed.

Finally, in a ***Conclusion*** section, the Examiner stated, "Applicant's amendment necessitated the new ground(s) of rejection presented in this Office

Action. Accordingly, **THIS ACTION IS MADE FINAL**". However, ***for the record***, Applicant made ***NO*** amendments in the Previous Response to necessitate "new ground(s) of rejection". Therefore, the Examiner's decision to make the Present Action final cannot be predicated on "Applicant's amendment", contrary to the Examiner's statement. Furthermore, given the "new ground(s) of rejection" presented for the first time in the Present Action when ***no amendment has been made*** by Applicant, Applicant respectfully submits that the finality of the Present Action ***is premature and should be withdrawn***. Reconsideration and withdrawal of the finality of the Present Action are respectfully requested.

In summary, Claims 1-25 were pending. Claims 12-20 were allowed, Claims 1-8, 11 and 21-25 were rejected, and Claims 9 and 10 were objected to but deemed allowable if rewritten in independent form. New Claims 26 and 27 are added. Applicant submits that 1-11 and 21-27 are in condition for allowance. It is respectfully requested that Claims 1-11 and 21-27 be allowed along with allowed Claims 12-20, and that the application be passed to issue at an early date.

Should the Examiner's action be other than allowance, the undersigned respectfully requests a telephone call from the Examiner to discuss further consideration that would expedite the prosecution of the application. Furthermore, should the Examiner have any questions regarding the above, please contact the undersigned, J. Michael Johnson, Agent for Applicant, at telephone number (775) 849-3085.

Respectfully submitted,
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